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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/512,267	02/24/2000	Woon-Yong Park	06192.0100	5968

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EXAMINER

KUMAR, SRILAKSHMI K

ART UNIT	PAPER NUMBER
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2675

DATE MAILED: 02/11/2003

11

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/512,267

Applicant(s)

PARK ET AL.

Examiner

Srilakshmi K. Kumar

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 November 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-7, 9-15 and 17-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9-15, 17-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                             | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Response to Amendment***

The following action is in response to Amendment B, filed November 25, 2002. Claims 8 and 16 have been cancelled. Claims 1, 4, 9, 12, 17 and 19 have been amended. Claims 21-23 are newly added.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6, 9, 12, 15, and 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US 6,229,516) in view of Konoue et al (JP03125187).

As to independent claim 1, Kim et al disclose a liquid crystal display, comprising;

a first gate line block including a plurality of first gate lines transmitting scanning signals, said first gate line block scanning in a first direction (Fig. 2, items 22 upper gate, G1 to Gm);

a second gate line block including a plurality of second gate lines transmitting scanning signals, said second gate line block scanning in a second direction (Fig. 2, items 24 lower gate, Gm+1 to G2m);

a plurality of first data lines transmitting image signals and crossing the first gate lines of said first gate line block (Fig. 2, item 12);

a plurality of second data lines transmitting image signals and crossing the second gate lines of said second gate line block (Fig. 2, item 14);

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a plurality of pixels configured in a matrix pattern and defined by the gate lines and the data lines, said pixels including switching elements coupled to the gate lines and the data lines (Fig. 2, col. 4, lines 15-29);

Kim et al do not disclose where the first direction is opposite to the second direction and the first data lines are separated from the second data lines. Konoue et al disclose a display device and scanning method for display device, where in Fig. 2a (on the Japanese Patent) and the Constitution on page 1, the screen is divided into upper and lower parts A and B, where the first scanning direction is opposite to the second scanning direction as shown by the solid arrowed lines. It would have been obvious to one of ordinary skill in the art to combine Kim et al with that of Konoue et al as the system of Konoue et al is shown to improve the continuity of an image at the border of each block in a display area and to preclude deterioration in picture quality.

Kim et al do not disclose wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a last gate line to a first gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction of the first gate line to a last gate line of second gate line block. Konoue et al disclose a display device and scanning method for display device, where in Fig. 2a (on the Japanese Patent) and the Constitution on page 1, the screen is divided into upper and lower parts A and B, wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a last gate line to a first gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction of the first gate line to a last gate line of second gate line block as shown by the solid arrowed lines. It would have been obvious to one of ordinary skill in

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the art to combine Kim et al with that of Konoue et al as the system of Konoue et al is shown to improve the continuity of an image at the border of each block in a display area and to preclude deterioration in picture quality.

As to independent claim 4, limitations of claim 1, and further comprising, a first frame memory (Fig. 2, item 42) that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the first data driver in synchronization with the read clock signals (Fig. 2, and col. 4, lines 30-36, col. 7, lines 22-47);

a second frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the second data driver in synchronization with the read clock signals (Fig. 2, and col. 4, lines 30-36, col. 7, lines 22-47);.

As to independent claims 12 and 17, see limitations of claims 1 and 4.

As to independent claims 19 and 21, limitations of claims 1, 4, and 12, further comprising, wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a first gate line to a last gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction of the last gate line to a first gate line of second gate line block. Kim et al do not disclose wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a first gate line to a last gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction of the last gate line to a first gate line of second gate line block. Konoue et al disclose a display device and scanning method for display device, where in Fig. 2a (on the Japanese Patent) and the Constitution on page 1, the screen is divided into upper and lower parts A and B, wherein

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the scanning signals are sequentially supplied to said first gate line block in a direction from a first gate line to a last gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction of the last gate line to a first gate line of second gate line block as shown by the dotted arrowed lines. It would have been obvious to one of ordinary skill in the art to combine Kim et al with that of Konoue et al as the system of Konoue et al is shown to improve the continuity of an image at the border of each block in a display area and to preclude deterioration in picture quality.

As to dependent claims 2, 5 and 22, limitations of claims 1, 4 and 21, respectively, and further comprising wherein the number of the first gate lines is equal (Fig. 1, items G1 to Gm, Gm+1 to G2m, and col. 4, lines 8-10).

As to dependent claims 3, 6 and 23, limitations of claims 2, 5 and 22, respectively, and further comprising wherein the first gate lines and the second gate lines are simultaneously scanned, col. 7, lines 34-44).

As to dependent claims 9 and 13, limitations of claims 4 and 12, respectively, and further comprising, wherein the first frame memory outputs the image signals, which are written in opposite order from the image signals to be provided to the first data lines, to the first data driver, and the second frame memory outputs the image signals which are written in identical order from the image signals to be provided to the second data lines, to the second data driver ((Fig. 2, and col. 4, lines 30-36, col. 7, lines 22-47)

As to dependent claims 18 and 20, see limitations of claims 1, 4, 12, 17 and 19.

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3. Claims 7, 10, 11, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,229,516) in view of Konoue et al (JP03125187) as applied to claims 1, 4, and 12, above, and further in view of Tanioka et al. (US 5,093, 655).

As to dependent claim 7, limitations of claim 5, and further comprising wherein polarities of the data voltages supplied to the pixels coupled to adjacent gate lines of said first gate line block are opposite to each other with respect to the common voltage, and the polarities of the data voltages supplied to the pixels coupled to the neighboring gate lines of said second gate line block are opposite to each other with respect to the common voltage. Kim et al do not disclose the polarities.

Tanioka et al disclose in Fig. 1, items 60 and 70 and col. 4, lines 13-26, wherein the polarities of the data voltages supplied to the pixels coupled to adjacent gate lines are opposite to each other. It would have been obvious to one of ordinary skill in the art to incorporate the polarity system of Tanioka et al into that of Kim et al. To reverse polarity is advantageous as it reduces flickers of the entire picture face as disclosed by Tanioka et al in col. 2, lines 43-49.

As to dependent claims 10, 11, 13 and 14, see limitations of claim 7, above.

#### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1, 4, 12, 17, 19 and 21 have been considered but are moot in view of the new ground(s) of rejection.

As to independent claims 1, 4, 12, 17, 19 and 21, the limitations of wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a last gate line to a first gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction of the first gate line to a last gate line of second gate line block and of

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wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a first gate line to a last gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction of the last gate line to a first gate line of second gate line block are clearly shown by Konoue et al as is described in the above rejection.

Konoue et al, in Fig. 2a, disclose where the screen is divided into upper and lower portions where the scanning directions are shown to be in opposite directions whether in “last to first and first to last” depicted by the solid arrows or “first to last and last to first” depicted by the dotted arrows.

### ***Conclusion***

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**Or faxed to:**

(703) 308-9051, (for formal communications intended for entry)

**Or:**

(703) 308-6606 (for informal or draft communications, please label

“PROPOSED” or DRAFT”)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive,

Arlington, VA, Sixth Floor (Receptionist)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 703 306 5575. The examiner can normally be reached on 8:00 am to 5:30 pm alternate Fridays off.



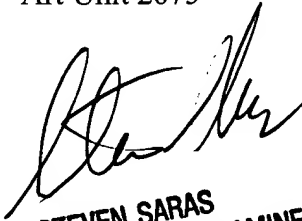
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703 305 9720. The fax phone numbers for the organization where this application or proceeding is assigned are 703 306-0377 for regular communications and 703 308 9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 4700.

Srilakshmi K. Kumar  
Examiner  
Art Unit 2675

SKK  
February 8, 2003



**STEVEN SARAS**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2600**